A2 concl'd

which a substrate bias is applied in a reverse direction by a potential in said well region.

REMARKS

The multiple dependencies have been eliminated from Claims 8-11 to avoid the surcharge for multiple dependent claims, see the accompanying hand-marked version. Claims 39-42 correspond to the dependencies eliminated from Claims 8-11.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:pdh

Miles & Stockbridge P.C.
1751 Pinnacle Drive
Suite 500
McLean, VA 22102-3833
(703) 903-9000

May 16, 2001

said first logic is formed and a well region of the MIS transistor in which said second logic gate is formed are made common every conduction type.

7. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of potentials having a relatively small potential difference; and

a second logic gate using, as an operation power source, a second pair of potentials having a relatively large potential difference,

wherein each of said first and second logic gates has an MIS transistor, and a well region of the MIS transistor in which said first logic gate is formed and a well region of the MIS transistor in which said second logic gate is formed are electrically made conductive every conduction type.

8. (Amended) A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

9. (Amended) A semiconductor integrated circuit according to claim 6

[or 7], wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by the potential of said well region, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential of said well region.

(Amended)
10. A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of said well region, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in said well region.

(Amended)
11. A semiconductor integrated circuit according to claim 6 [or 7], wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential in said well region.

12. A semiconductor integrated circuit comprising:

a first logic gate using, as an operation power source, a first pair of a high potential and a low potential; and

ABSTRACT

Disclosed is a semiconductor integrated circuit realizing improved operating speed, reduced power consumption in an active mode, reduced power consumption in a standby mode, and reduced area of a chip. A first logic gate using a first pair of potentials VDDL, VSSL having a relatively small potential difference as an operation power source and a second logic gate using a second pair of potentials VDDH, VSSH having a relatively large potential difference as an operation power source commonly use substrate potentials VBP, VBN of MIS transistors. The second logic gate has a relatively high driving capability, and the first logic gate can operate on relatively low power. The MIS transistor has a threshold voltage which increases by a reverse substrate bias and decreases by a forward substrate bias. By commonly using the substrate potential, even in the case where different substrate bias states are generated at both of the logic gates, MOS transistors of the logic gates can be formed in the common well region.